REMARKS

Claims 1-41 are pending in this application. Claims 1-5, 7 and 39-41 stand rejected, claims 8-38 are allowed, and claim 6 is objected to. Claims 10 and 28 have been amended to be consistent with FIG. 8 and paragraph [0043], which illustrates that the signal generated in the first refresh section has a shorter period (tp2) than the period (tp3) of the signal generated in the second refresh section, i.e., tp2 < tp3.

It is noted that the Examiner rejected dependent claim 40, while allowing claim 26 on which claim 40 depended. Claim 40, by amendment, now depends on allowable claim 26, and therefore is allowable. Applicant therefore presumes that the Examiner meant to reject claims 1-5, 7, 39 and 41 only. Reconsideration of the application is respectfully requested.

Allowable Subject Matter

Applicant appreciates the indication that claims 8-38 are allowed and presumes that claim 40 is also allowed because it depends on allowable claim 26. Applicant also appreciates the indication that claim 6 is objected to as being dependent upon the rejected based claim, but would be allowable if rewritten in independent form. However, it is respectfully submitted that claims 1-5, 7, 39 and 41 are also allowable in view of the foregoing remarks.

A Description of an Example Embodiment

Fig. 1 discloses an example embodiment of the present invention. As shown, a chip select buffer circuit 150 may process an external chip select signal XCSB into an internal chip select signal ICSB. In response to the internal chip select signal ICSB and an oscillation signal POSC, a detector circuit 60 may produce a flag signal POSC_CSB. An example embodiment may also include an oscillation circuit 170 that may produce an oscillation signal POSC having a period, which may vary based on the given mode of operation indicated by a flag signal POSC_CSB. A refresh pulse generator circuit 180 may produce a refreshed pulse signal PRFHTD in response to the oscillation signal POSC. The refresh pulse signal PRFHTD may have the same period as the oscillation signal POSC and/or may have a pulse width differing from the pulse width of the oscillation signal POSC. In response to the refresh pulse signal, a word line enable circuit 190 may produce a word line enable signal PWA, which may vary according to the internal chip select signal ICSB. The pulse width of the word line enable signal PWA may vary depending on whether the semiconductor memory device 100 is in standby mode or active mode and/or on whether the device is in the first or second self-refresh section (Fig. 8). The word line enable signal PWL may feed into a row decoder circuit 120, which may select word lines WL0 to WLm in response to addresses output from an address generator circuit 130 or from an address buffer circuit 140.

Prior Art Rejections

35 U.S.C. §102(b) Kim Rejection

Claims 1-3, 7, 39, and 41 stand rejected under 35 U.S.C. §102(b) as being anticipated by Kim et al. (U.S. Patent No. 5,461,591). Applicants respectfully traverse this art ground of rejection.

Fig. 5 is a block diagram showing the Back-Bias Voltage Generator according to Kim's preferred embodiment. Fig. 6 is a detailed circuit diagram of Fig. 5 (Col. 4, Ln. 59 – Col. 5, Ln. 14). Switches SW1, SW2, and SW3 in Fig. 5 have incoming signals S1, S2, and S3. These incoming signals correspond to /RAS1 (row address signal), /SAEN (bit line sense amplifier enable signal) and BBSEN (back bias voltage detecting signal) in Fig. 6. The switches serve as by-pass circuits to vary the oscillation frequency of the back bias voltage generator as shown in Fig. 4 and Fig. 7 (element c). Fig. 7, provides an operation timing chart for the various signals in Fig. 6, including Oscillator Signal (c) and output back-bias Voltage Vbb. As is evident from the signals produced by the disclosed Back-Bias Voltage Generator, **output signal Vbb does not pulsate or oscillate**.

In making the outstanding rejection, the Examiner modifies the Back-Bias Voltage Generator in the preferred embodiment, into an internal voltage generator disclosed as an alternate embodiment in Col. 3, Ln. 64 – Col. 4, Ln. 4. To combine the internal high voltage generator embodiment (Col. 3, Ln. 64 – Col. 4, Ln. 4) with the back-bias voltage generator embodiment (Figs. 5 and 6; as done by the Examiner), the 3 input signals (S1, S2, and S3) would be reduced to

2 input signals. New S1 would be designated as the internal high voltage detecting signal, and New S2 would be designated for the word line enable signal.

In Figs. 4 and 7, Kim et al. only teaches an oscillator signal (element c in Fig. 7) produced by an oscillator circuit. In Col. 4, Ln. 59 – Col. 5, Ln. 14, Kim et al. discloses the elements of the back-bias voltage generator of the preferred embodiment, Kim does **not teach the use of a control circuit for controlling the oscillator circuit AND the word line enable circuit**. Furthermore, the oscillator disclosed by Kim et al. **uses the word line enable signal as input**, and therefore cannot disclose generating a word line enable signal in response to the oscillation signal. Applicant, therefore, submits that Kim et al. cannot teach or suggest "a word line enable circuit for **generating a word line enable signal in response to the oscillation signal**; and a **control circuit for controlling the oscillator circuit and the word line enable circuit** so that **the pulse width of the word line enable signal is widened** as operation mode of the memory device changes from an active mode to a standby mode" as recited in claim 1. Applicant further submits that, Kim et al. cannot teach or suggest "the method comprising controlling the length of a period of the oscillation signal generated by the oscillation circuit and **the pulse width of a word line enable signal** generated by the word line enable circuit in response to the oscillation signal **based on a change in mode of operation of the device**." as recited in claim 39.

For the reasons stated above, claims 1 and 39 are patentable over Kim et al. Furthermore, Applicants submit that, at least for the reasons set forth above, claims 2-7 and 41 are also patentable over Kim et al. because they depend on patentable claims 1 and 39.

35 U.S.C. §102(e) Takita Rejection

Claims 1-5 and 7 stand rejected under 35 U.S.C. §102(e) as being anticipated by Takita et al. (U.S. Patent No. 6,628,564). Applicants respectfully traverse this art ground of rejection.

In Fig. 21, Takita discloses a block diagram of a basic embodiment of a semiconductor device including a negative potential generating circuit for setting the reset potential of a word line to a negative potential (Col. 6, Ln. 65-67 – Col. 7, Ln. 2). Fig. 21 includes a reset level control circuit 600 connected to a word line reset level generating circuit 400. The word line reset level generating circuit 400 connects to a memory cell array 100, a word line driver 200, and a row decoder 300, as well as a reset level detecting circuit 500.

Fig. 25 shows a block diagram of the word line reset level generating circuit 400. As shown, the word line reset level generating circuit 400 includes an oscillation circuit 210, a level converting circuit 220, a capacitor drive circuit 230, a capacitor 240 and a rectifier 250 connected in series. The output of the word line reset level generating circuit 400, vnwℓ represents the steady negative voltage level vnwℓ used to establish the current state of the memory cell array; the state being either standby, active or intermediate (Col. 26 Lns. 15-35; Col. 30, Lns. 50-60).

Fig. 32 provides a timing diagram for explaining the control operation of the word line reset level generating circuit 400 and the three states for the memory cell array. It is clear from the diagram that the **only oscillating signal** output is the signal OS output by the oscillation circuit 210. When the negative voltage level vnwℓ is between V4 and V5, the oscillator output signal OS becomes active so long as the bank selection signal BA is high. When the bank selection signal BA drops, a control oscillation signal EN and the oscillator output signal OS both dampen. In the case where negative voltage level vnwℓ is higher than V5, the oscillator output signal OS continues regardless of the bank selection signal BA.

Takita et al. teaches a reset level control circuit 600 controlling a word line reset level generating circuit 400, which produces a vnwℓ voltage. In Fig. 32, Takita only discloses that **oscillator output signal OS is an oscillating signal**. The output of the word line reset level generating circuit 400 is not a pulse signal, as is evident by the fact that it passes through a rectifier. Furthermore, in Fig. 32, when the oscillator output signal OS is activated, it has a **constant pulse width and constant period**. Applicant, therefore, submits that Takita cannot teach or suggest "a control circuit for controlling the oscillator circuit and the word line enable circuit so that **the pulse width of the word line enable signal is widened** as operation mode of the memory device changes from an active mode to a standby mode" as recited in claim 1. Applicant further submits that Takita cannot teach or suggest the "a method of controlling operation of a semiconductor memory device that includes an oscillation circuit and a word line

enable circuit, the method comprising **controlling the length of a period of the oscillation signal** generated by the oscillation circuit and **the pulse width of a word line enable signal** generated by the word line enable circuit in response to the oscillation signal **based on a change in mode of operation of the device**." as recited in claim 39.

For the reasons stated above, claims 1 and 39 are patentable over Takita. Furthermore, Applicant submits that, at least for the reasons set forth above, claims 2-6 and 41 are also patentable over Takita because they depend on allowable claims 1 and 39.

In view of the above remarks, Applicants further submit that neither Kim et al. nor Takita, either alone or in combination, teach or suggest the features of independent claims 1 or 39. Furthermore, claims 2-7, and 41 are also patentable because they depend on patentable claims 1 and 39.

Therefore, withdrawal of the outstanding rejections is respectfully requested.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of claims 1-41 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By _____ 45774
John A. Castellano, Reg. No. 35,094

P.O. Box 8910
Reston, Virginia 20195
(703) 668-8000

JAC/NMZ:lak